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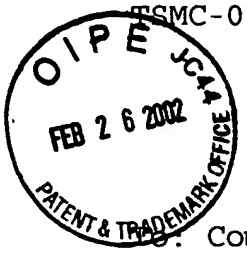

February 12, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 10/002,031 11/30/01

Yee-Chia Yeo, Chun-Chieh Lin,
Fu-Liang Yang, Chen Ming Hu

COMPLEMENTARY METAL OXIDE SEMI-CONDUCTOR TRANSISTOR TECHNOLOGY USING SELECTIVE EPITAXY OF A STRAINED SILICON GERMANIUM LAYER

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 15, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 2/15/02

U.S. Patent 5,534,713 to Ismail et al., "Complementary Metal-Oxide Semiconductor Transistor Logic Using Strained SI/SIGE Heterostructure Layers," describes the use of thick buffer layers, used with a SiGe layer.

U.S. Patent 5,019,882 to Solomon et al., "Germanium Channel Silicon MOSFET," discloses a Ge channel Si MOSFET process.

U.S. Patent 6,004,137 to Crabbe et al., "Method of Making Graded Channel Effect Transistor," discloses a SixGe1-x graded channel effect Tx.

U.S. Patent 5,985,703 to Banerjee, "Method of Making Thin Film Transistors," discloses a Tx using SixGe1-x layers.

U.S. Patent 5,241,197 to Murakami et al., "Transistor Provided with Strained Germanium Layer," discloses FET's with SixGe1-x layers.

U.S. Patent 5,981,345 to Ryum et al., "FI/SIGE MOSFET and Method for Fabricating the Same," discloses a SixGe1-x channel.

Sincerely,

Stephen B. Ackerman,
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